

## WHAT IS CLAIMED IS:

- 1           1. A data transfer system comprising:  
2           a plurality of first bus devices, at least one first bus  
3 device being a first bus data supplying device capable of  
4 supplying data, at least one first bus device being a first  
5 bus data receiving device capable of receiving data and at  
6 least one first bus device being a first bus master device  
7 capable of requesting and controlling data transfer;  
8           a first data bus connected to each of said plurality of  
9 first bus devices and capable of transferring data from a  
10 first bus data supplying device to a first bus data receiving  
11 device under control of a first bus master device;  
12           a plurality of second bus devices, at least one second  
13 bus device being a second bus data capable of supplying device  
14 capable of supplying data, at least one second bus device  
15 being a second bus data receiving device capable of receiving  
16 data and at least one second bus device being a second bus  
17 master device capable of requesting and controlling data  
18 transfer;  
19           a second data bus connected to each of said plurality of  
20 second bus devices and capable of transferring data from a  
21 second bus data supplying device to a second bus data  
22 receiving device under control of a second bus master device;  
23           a bus bridge connected to said first data bus and said  
24 second data bus, said bus bridge capable of supplying data to  
25 said first bus, receiving data from said first bus, supplying  
26 data to said second bus, receiving data from said second bus,  
27 not capable of controlling data transfer on said first bus and  
28 capable of controlling data transfer on said second bus, said  
29 bus bridge including

30           an address first-in-first-out memory having a  
31           predetermined number of entries including an input  
32           connected to said first bus and an output connected to  
33           said second bus, and  
34           a data first-in-first-out memory having said  
35           predetermined number of entries including an input  
36           connected to said first bus and an output connected to  
37           said second bus.

1           2. The data transfer apparatus of claim 1, further  
2           comprising:

3           a first bus arbiter connected to each of said at least  
4           one first bus master device and said first bus, said first bus  
5           arbiter granting control of data transfer on said first bus to  
6           one and only one first bus master; and

7           a second bus arbiter connected to each of said at least  
8           one second bus master device, said second bus and said bus  
9           bridge, said second bus arbiter granting control of data  
10          transfer on said first bus to one and only one of the set of  
11          devices including each second bus master and said bus bridge.

1           3. The data transfer system of claim 1, wherein:

2           at least one first bus device being a first bus  
3           supplying/receiving device capable of both supplying data to  
4           said first bus and receiving data from said first bus.

1           4. The data transfer system of claim 3, wherein:

2           at least one first bus supplying/receiving device  
3           consists of a central processing unit which is further capable  
4           of controlling data transfer.

1           5. The data transfer system of claim 3, wherein:  
2           at least one first bus supplying/receiving device  
3 consists of a direct memory access unit which is further  
4 capable of controlling data transfer.

1           6. The data transfer system of claim 3, wherein:  
2           at least one first bus supplying/receiving device  
3 consists of a memory which is not capable of controlling data  
4 transfer.

1           7. The data transfer system of claim 3, wherein:  
2           at least one first bus supplying/receiving device  
3 consists of a central processing unit which is further capable  
4 of controlling data transfer; and  
5           said bus bridge further including at least one control  
6 register accessible by said central processing unit, said bus  
7 bridge setting a predetermined buffer full bit of said at  
8 least one control register when said address  
9 first-in-first-out memory and said data first-in-first-out  
10 memory are full.

1           8. The data transfer system of claim 3, wherein:  
2           at least one first bus supplying/receiving device  
3 consists of a central processing unit which is further capable  
4 of controlling data transfer; and  
5           said bus bridge further operable to generate an interrupt  
6 of said central processing unit when said address first-in-  
7 first-out memory and said data first-in-first-out memory are  
8 full.

1        9. The data transfer system of claim 8, wherein:  
2        said bus bridge further including at least one control  
3        register accessible by said central processing unit including  
4        a buffer full interrupt enable bit, said bus bridge  
5        selectively generating an interrupt of said central processing  
6        unit when said address first-in-first-out memory and said data  
7        first-in-first-out memory are full and said buffer full  
8        interrupt enable bit has a predetermined digital state.

1        10. The data transfer system of claim 3, wherein:  
2        at least one first bus supplying/receiving device  
3        consists of a central processing unit which is further capable  
4        of controlling data transfer; and  
5        said bus bridge further including at least one control  
6        register accessible by said central processing unit, said bus  
7        bridge setting a predetermined buffer empty bit of said at  
8        least one control register when said address first-in-first-  
9        out memory and said data first-in-first-out memory are empty.

1        11. The data transfer system of claim 3, wherein:  
2        at least one first bus supplying/receiving device  
3        consists of a central processing unit which is further capable  
4        of controlling data transfer; and  
5        said bus bridge further operable to generate an interrupt  
6        of said central processing unit when said address first-in-  
7        first-out memory and said data first-in-first-out memory are  
8        empty.

1        12. The data transfer system of claim 11, wherein:  
2        said bus bridge further including at least one control  
3        register accessible by said central processing unit including

4 a buffer full interrupt enable bit, said bus bridge  
5 selectively generating an interrupt of said central processing  
6 unit when said address first-in-first-out memory and said data  
7 first-in-first-out memory are full and said buffer full  
8 interrupt enable bit has a predetermined digital state.

1 13. The data transfer system of claim 3, wherein:  
2 at least one first bus supplying/receiving device  
3 consists of a central processing unit which is further capable  
4 of controlling data transfer; and  
5 said bus bridge further including at least one control  
6 register accessible by said central processing unit, said bus  
7 bridge setting a predetermined buffer full bit of said at  
8 least one control register when an entry in said address  
9 first-in-first-out memory and said data first-in-first-out  
10 memory has been overwritten.

1 14. The data transfer system of claim 3, wherein:  
2 at least one first bus supplying/receiving device  
3 consists of a central processing unit which is further capable  
4 of controlling data transfer; and  
5 said bus bridge further operable to generate an interrupt  
6 of said central processing unit when an entry in said address  
7 first-in-first-out memory and said data first-in-first-out  
8 memory has been overwritten.

1 15. The data transfer system of claim 14, wherein:  
2 said bus bridge further including at least one control  
3 register accessible by said central processing unit including  
4 a buffer full interrupt enable bit, said bus bridge  
5 selectively generating an interrupt of said central processing

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6 unit when an entry in said address first-in-first-out memory  
7 and said data first-in-first-out memory has been overwritten  
8 and said buffer full interrupt enable bit has a predetermined  
9 digital state.

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